Design of 4-bit Adder and Subtracter circuits using a ripple carry logic and carry look-ahead logic.

By:

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Problem statement:

Our groups was to:

1. Design a 4-bit adder circuits using a ripple carry logic and
   carry look-ahead logic and

2. Design a 4-bit subtraction circuit using ripple carry logic

Design goals

1. Optimize the design to implement the function using the smallest number of gate count.

2. Find the worst case gate delay in implementing the two adder designs.

3.Compare the two designs and summarize the results.

Implementation

1. Implement the whole design in Mentor Graphics using Schematic
capture tool suite.

2. Simulate the two design using the input stimulus list provided

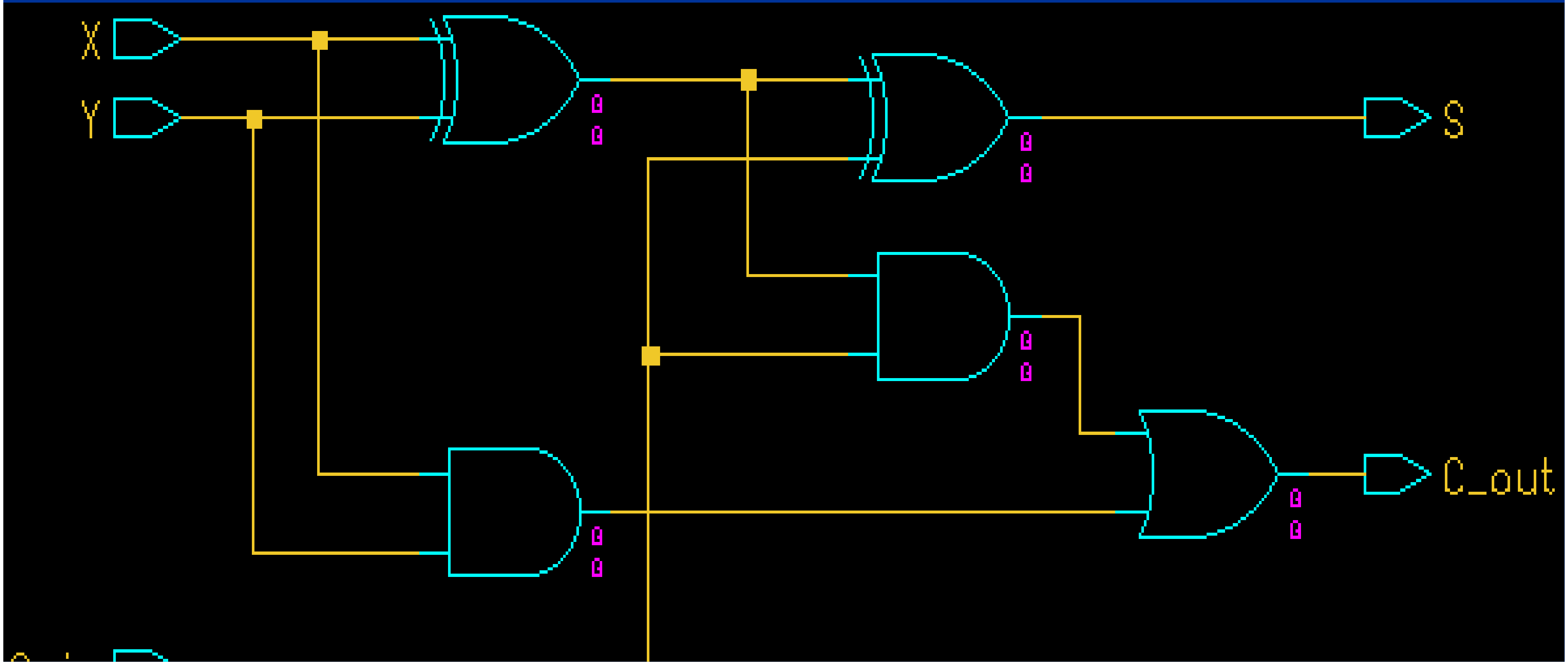
Full Adder

-A Full Adder is a circuit that adds two binary values with respect to the Carry Input. A full subtracter is just a Full Adder with certain inputs complemented

The formula for a full adder is $X \oplus Y \oplus$ Carry in.

Full Adder

Which lead our group to this logic circuit:



Ripple Carry

-A ripple carry circuit can be thought of as serial data processing. Once an action is done, it is carried to the next stage. This is somewhat slower than other methods.

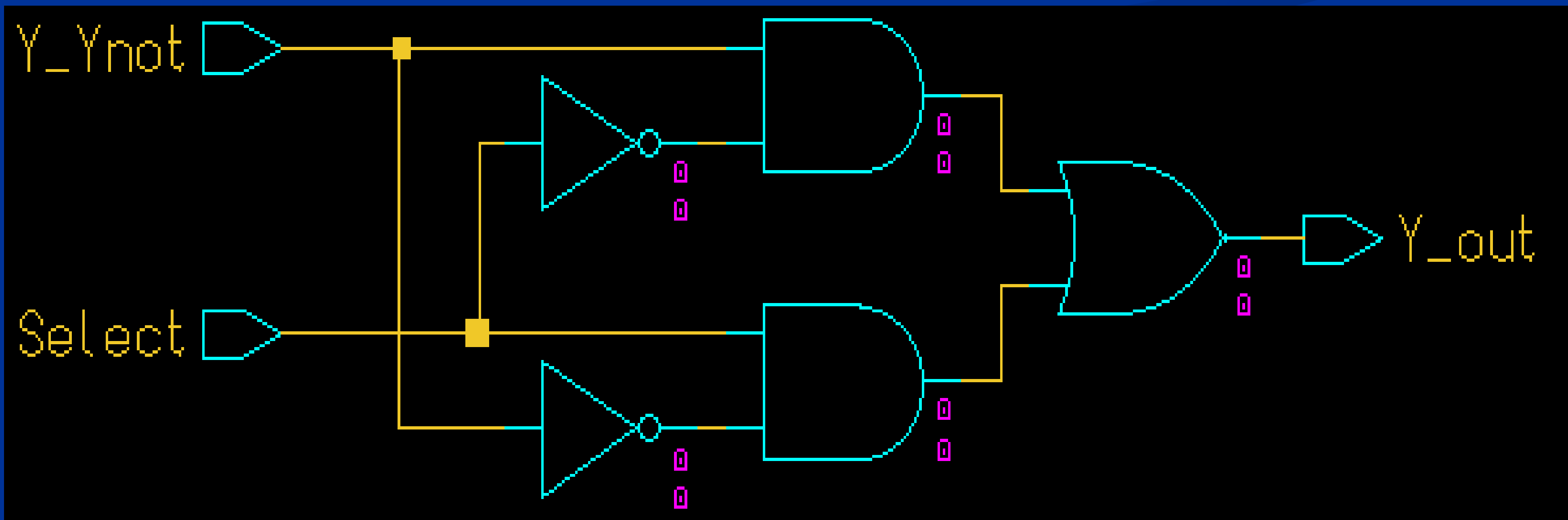
Carry Look-Ahead

-Carry Look-Ahead logic can be thought of as parallel data processing. It does the same thing that the Ripple Carry does, but it does it all at the same time.

With the project requirements taken care of, Our team decided to add extra capabilities to our designs.

Multiplexer

A multiplexer selects one of the input signals to be propagated to the output.

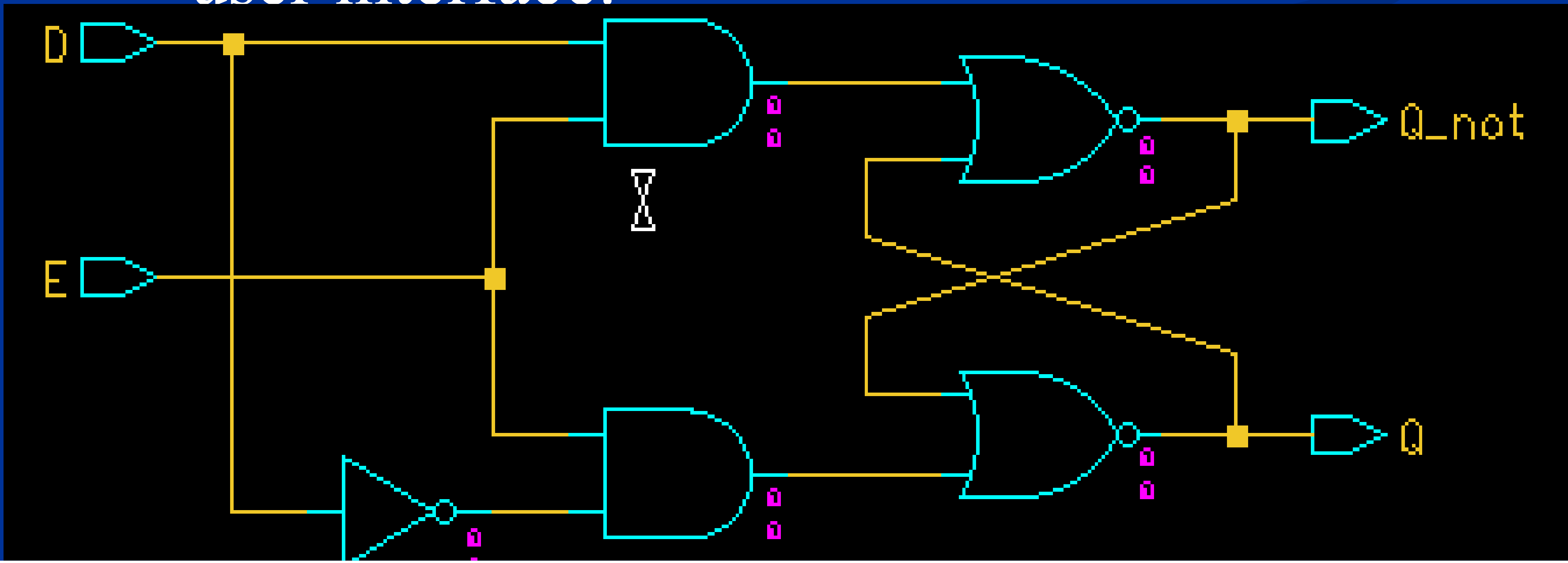


Multiplexer

This allows the team to combine our Ripple Carry Adder and Ripple Carry Subtracter circuits.

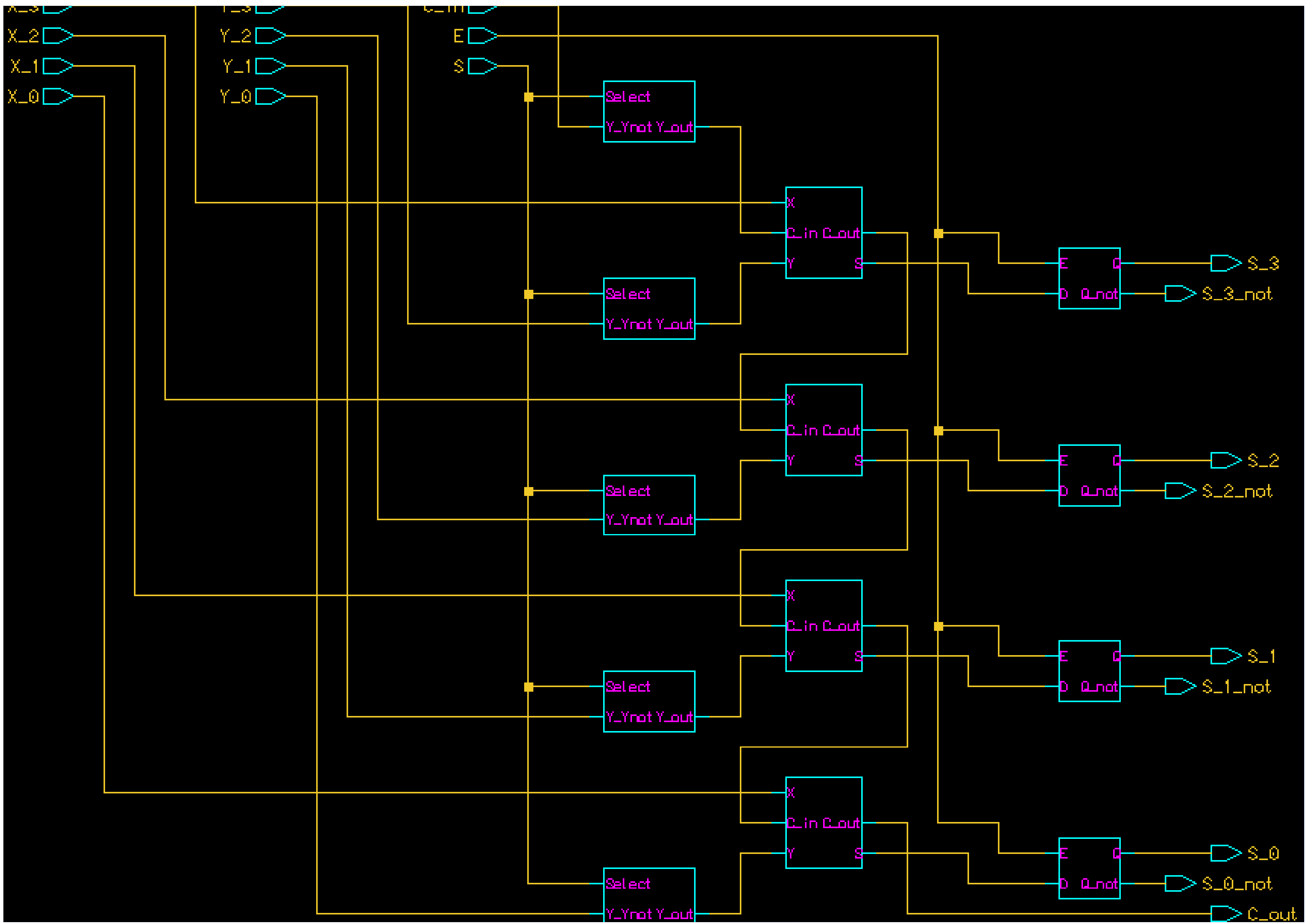
D-Latch

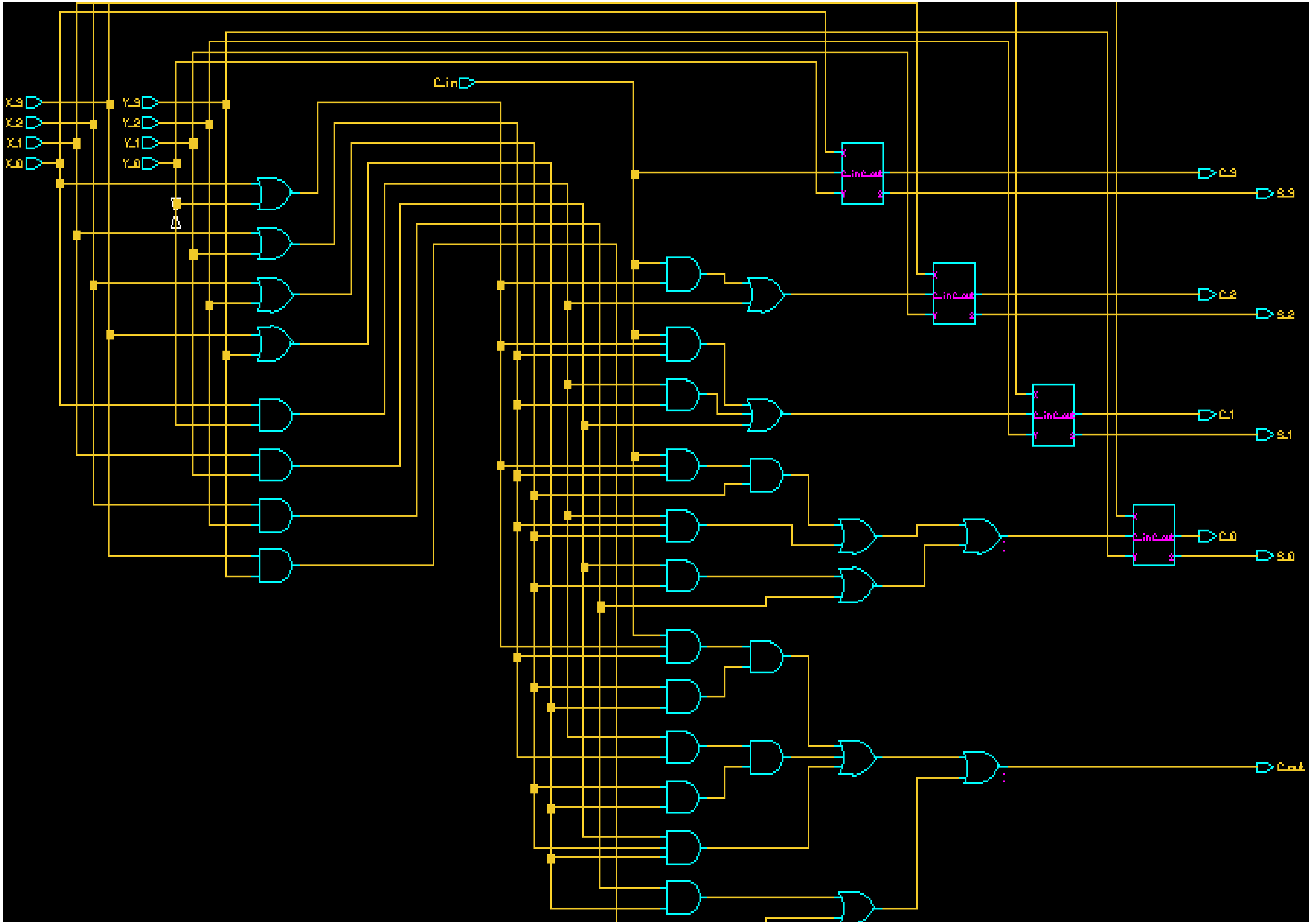
A D-Latch is a memory storage circuit. It holds a value until the Enable pin is reset, this allows for an optional addition to the circuit which is a simple user interface.



Final Products

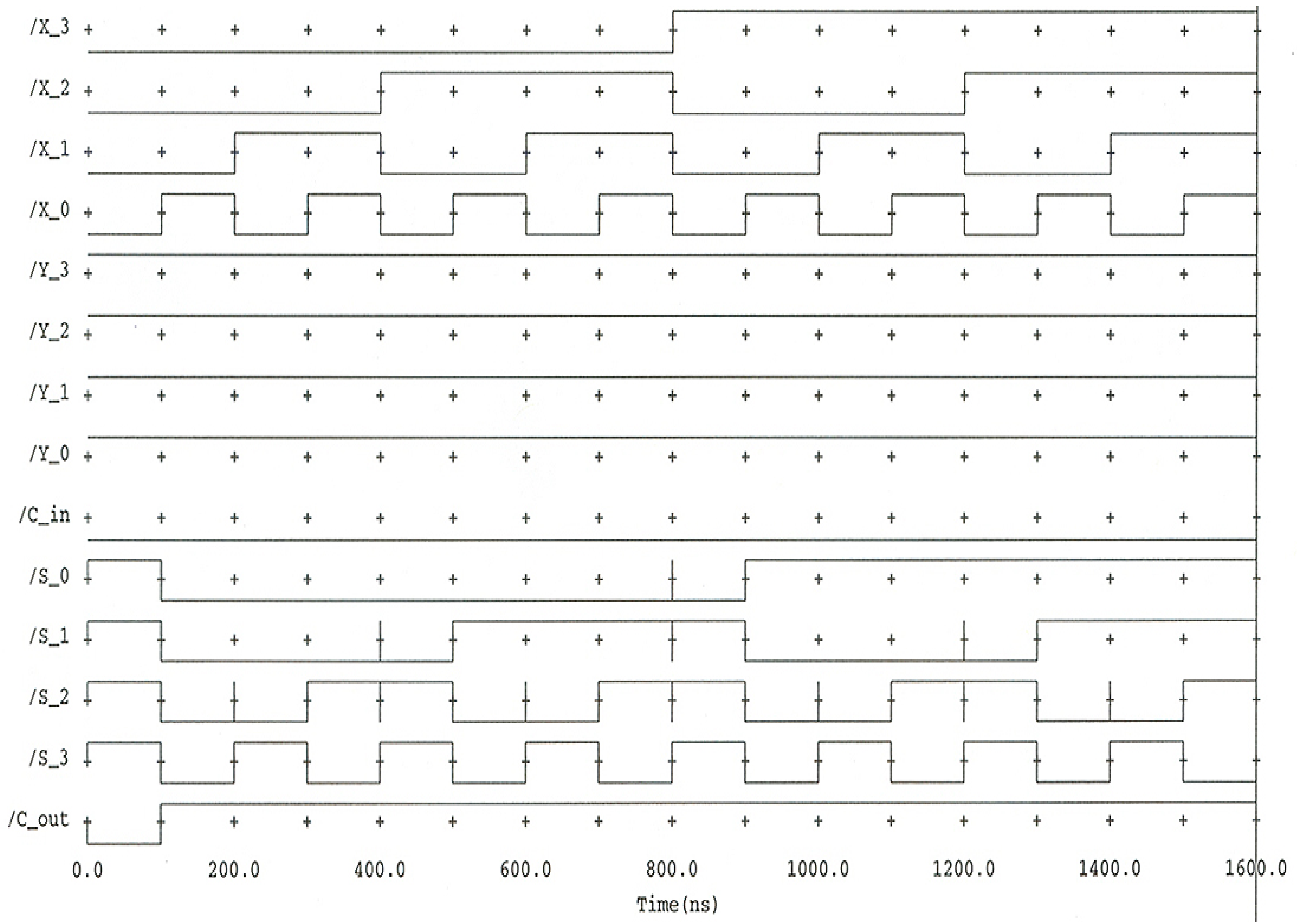
The final products are a Ripple Carry Full Subtracter/Subtracter with memory (for a simple user interface that may be added later if desired,) and a Carry Look-Ahead Full Adder.

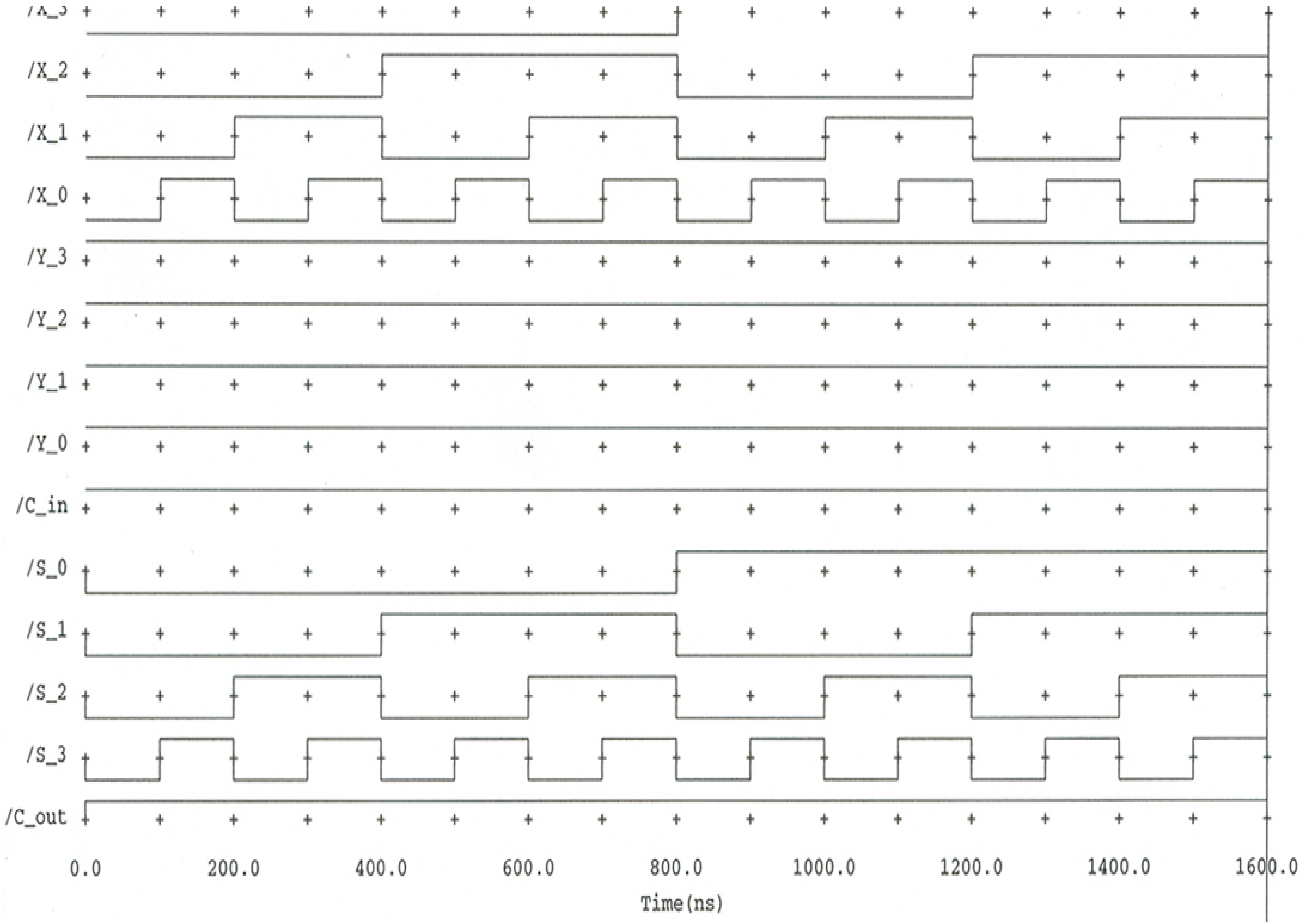

X_2
X_1
X_0
Y_2
Y_1
Y_0
E
S
Select
Y_Ynot Y_out
X
C_in C_out
Y
S
E
Q
D
Q_not
S_3
S_3_not
S_2
S_2_not
S_1
S_1_not
S_0
S_0_not
C_out



X_3
X_2
X_1
X_0
Y_3
Y_2
Y_1
Y_0
Cin
C3
S3
C2
S2
C1
S1
C0
S0
Cout

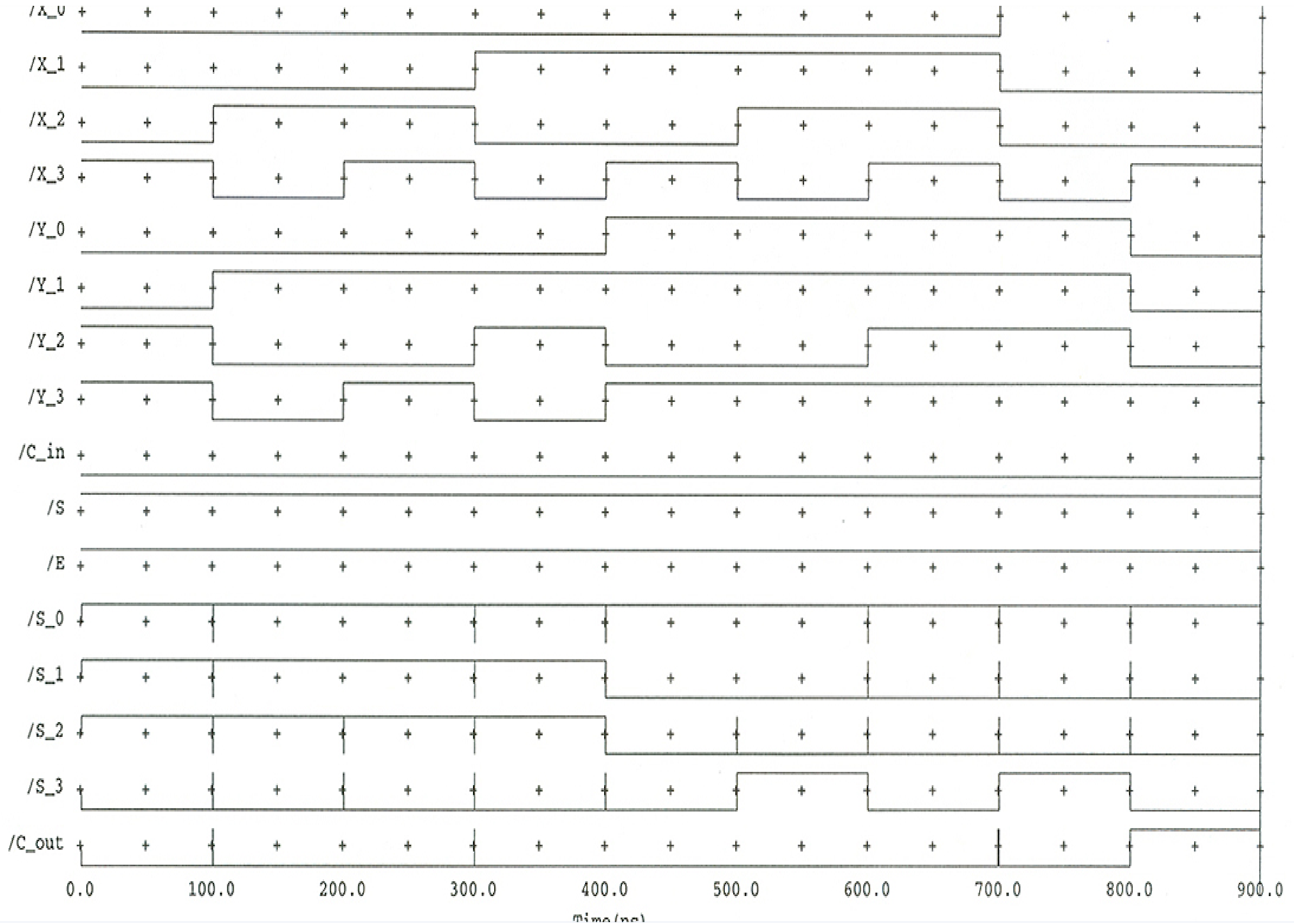
Outputs for the adders

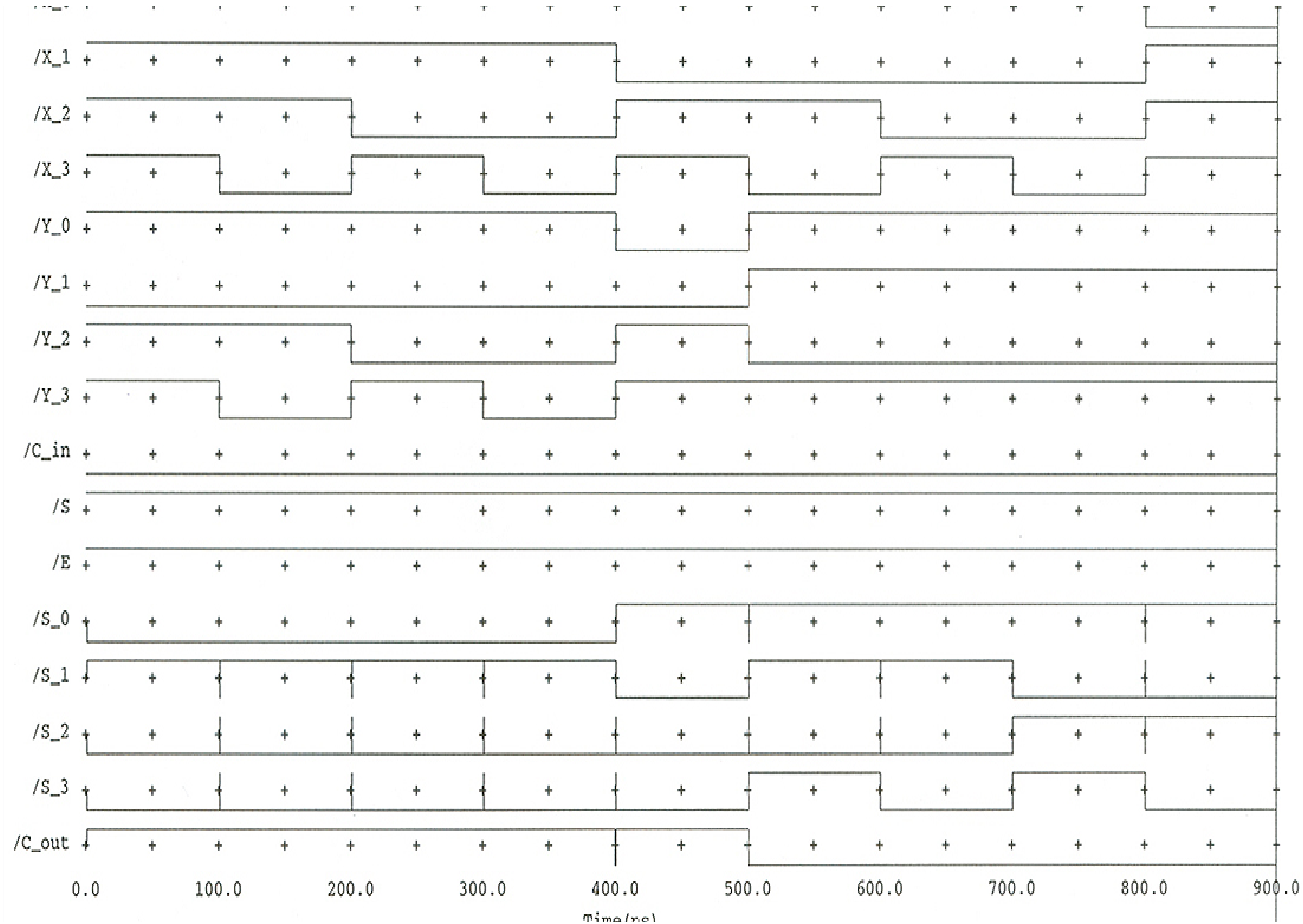

/X_3
/X_2
/X_1
/X_0
/Y_3
/Y_2
/Y_1
/Y_0
/C_in
/S_0
/S_1
/S_2
/S_3
/C_out
0.0
200.0
400.0
600.0
800.0
1000.0
1200.0
1400.0
1600.0
Time(ns)



/X_2
/X_1
/X_0
/Y_3
/Y_2
/Y_1
/Y_0
/C_in
/S_0
/S_1
/S_2
/S_3
/C_out
0.0
200.0
400.0
600.0
800.0
1000.0
1200.0
1400.0
1600.0
Time(ns)

Outputs for the subtracter


/X_0
/X_1
/X_2
/X_3
/Y_0
/Y_1
/Y_2
/Y_3
/C_in
/S
/E
/S_0
/S_1
/S_2
/S_3
/C_out
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
900.0
Time(ns)


/X_1
/X_2
/X_3
/Y_0
/Y_1
/Y_2
/Y_3
/C_in
/S
/E
/S_0
/S_1
/S_2
/S_3
/C_out
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
900.0